

Arm Research Summit 2017

Research Starter Kit

System Modeling using gem5

An aerial photograph of a group of cyclists riding on a cobblestone path. The image is overlaid with a light blue grid pattern. The word 'arm' is written in white lowercase letters on the left side of the image.

arm

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Arm Research Summit
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Research Enablement

Research Enablement

Mass Research Enablement

- Provide lightweight processes to access Arm IP
- Entice “Arm-affiliated” research at universities worldwide, Identify opportunities
- Develop Research Starter Kits and Services
- Increase efficiency (one-to-many)

Research Starter Kits

- Equivalent of Education Kits in Research
- Software packages, models, tools, and hardware prototypes to enable speedy migration/adoption of Arm and partner-based technologies at universities worldwide

Areas of Focus

- SoC Design, Subsystems
- Simulation and Modeling
- Networking - IoT – Cloud
- Data Science – Machine Learning

System Modeling



Topics covered

<http://www.arm.com/ResearchEnablement/SystemModeling>

Arm System Modeling

- Introduction to gem5
- Using this Research Starter Kit
 - Requirements
 - Download and Build
- Simulating Arm in gem5
 - System Call Emulation (SE)
 - Full System (FS)
- gem5 Statistics

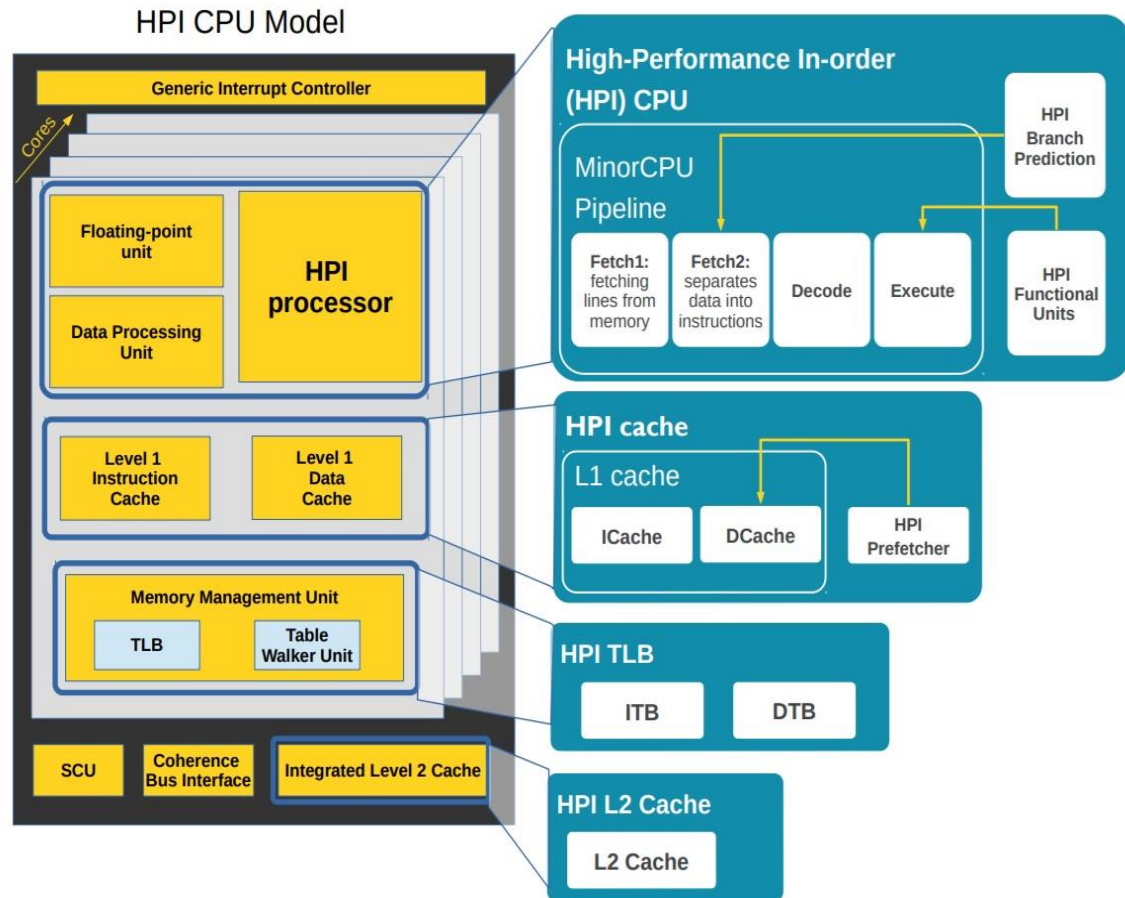
HPI Model

- In-order CPU Models in gem5
 - Memory access
 - AtomicSimpleCPU, TimingSimpleCPU, MinorCPU
- MinorCPU
 - Pipeline stages
- High-Performance In-order (HPI) CPU

Benchmarks (SE & FS)

- SE Mode
 - SingleSource workloads: the LLVM test-suite
- FS Mode
 - PARSEC 3.0
- Compiling FS Benchmarks
 - Cross-Compiling
 - Compiling on QEMU
- Running FS Benchmarks
 - Expanding the disk image

High-Performance In-order (HPI) Model



HPI

["HPI_BP", "HPI_ITB", "HPI_DTB", "HPI_WalkCache",
"HPI_ICache", "HPI_DCache", "HPI_L2", "HPI"]

- Processor pipeline
- Branch Predictor
- TLB
- L1 Cache
- L2 Cache

Research Starter Kit: *gem5* Official Repository

HPI core:

- The High-Performance In-order (HPI) CPU timing model is tuned to be representative of a modern in-order Armv8-A implementation.
- `gem5/configs/common/cores/arm/HPI.py`

SE Simulation Script:

- Simulation script for the Arm SE simulation (cpu type, cpu freq, num of cores, mem info, cmd to run, etc.)
- `gem5/configs/example/arm/starter_se.py`

FS Simulation Script:

- Simulation script for the Arm FS simulation (cpu type, cpu freq, num of cores, mem info, kernel, disk image, etc.)
- `gem5/configs/example/arm/starter_fs.py`

More information:

- <http://www.arm.com/ResearchEnablement/SystemModeling>

Research Starter Kit: *arm-gem-rsk* Git Repository

Documentation:

- 30-page document: gem5 basics, Arm HPI model, and benchmarks

Clone script:

- A script to download all the required materials: clones *gem5* and *arm-gem5-rsk* repositories

arm-gem5-rsk Wiki:

- A cheat sheet, containing all code and examples provided in the documentation

Parsec patches:

- Patches for compiling PARSEC for the gem5 Full-System simulation mode

Supporting scripts:

- A script to read the gem5 statistics, and a script for creating runscripts for PARSEC benchmarks